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Stylesheet Version v1.1.1

Claims

[c1] 1. A method of forming a high power device in wide-bandgap materials with reduced junction temperature, higher power density during operation and improved reliability at a rated power density, the method comprising:
adding a layer of diamond to a silicon carbide wafer to increase the thermal conductivity of the resulting composite wafer;
thereafter reducing the thickness of the silicon carbide portion of the composite wafer while retaining sufficient thickness of silicon carbide to support epitaxial growth thereon;
preparing the silicon carbide surface of the composite wafer for epitaxial growth thereon; and
adding a Group III nitride epitaxial layer to the prepared silicon carbide face of the wafer.

[c2] 2. A method according to Claim 1 comprising adding a Group III nitride heterostructure to the prepared silicon carbide face of the wafer.

[c3] 3. A method according to Claim 1 comprising growing the diamond layer on the C-face of the silicon carbide wafer and adding the heterostructure to the Si-face of

the wafer.

[c4] 4. A method according to Claim 1 comprising growing a polycrystalline layer of diamond.

[c5] 5. A method according to Claim 1 comprising depositing a diamond layer that is thick enough to support the added heterostructure while avoiding additional material that fails to provide further functional benefit.

[c6] 6. A method according to Claim 5 comprising adding a diamond layer that is between about 100 and 300 microns thick.

[c7] 7. A method according to Claim 1 wherein the step of preparing the SiC surface comprises polishing the SiC surface.

[c8] 8. A method according to Claim 1 wherein the step of reducing the thickness of the SiC portion comprises lapping and polishing the SiC portion.

[c9] 9. A method according to Claim 1 wherein the step of reducing the thickness of the silicon carbide portion comprises:
implanting the silicon carbide substrate at a predetermined depth in the silicon carbide to form an implanted layer within the silicon carbide prior to the step of de-

positing the diamond;
thereafter depositing the diamond; and
thereafter reducing the thickness of the silicon carbide portion by separating the silicon carbide at the implanted layer.

[c10] 10. A method according to Claim 9 comprising implanting the silicon carbide substrate with oxygen to form a layer of silicon dioxide and thereafter separating the silicon carbide at the silicon dioxide layer.

[c11] 11. A method according to Claim 9 comprising implanting the silicon carbide substrate with hydrogen and thereafter separating the silicon carbide at the hydrogen-implanted layer.

[c12] 12. A method according to Claim 1 comprising depositing the diamond on the silicon carbide by chemical vapor deposition.

[c13] 13. A method according to Claim 12 comprising depositing two layers of diamond that differ in properties from one another.

[c14] 14. A method according to Claim 1 comprising:
depositing a layer of semi-insulating diamond on a layer of semi-insulating silicon carbide to provide a semi-insulating substrate for high-frequency devices;

thereafter depositing a second layer of diamond on the semi-insulating layer to provide additional mechanical stability during wafer processing.

[c15] 15. A method according to Claim 14 comprising:
processing the wafer with the second diamond layer and thereafter removing portions of the second layer of diamond.

[c16] 16. A method according to Claim 1 comprising bonding the diamond to the silicon carbide.

[c17] 17. A method according to Claim 1 comprising adding a layer of a second material other than diamond to the diamond layer opposite the silicon carbide.

[c18] 18. A high power, wide-bandgap device that exhibits reduced junction temperature and higher power density during operation and improved reliability at a rated power density, said device comprising:
a diamond substrate for providing a heat sink with a thermal conductivity greater than silicon carbide;
a single crystal silicon carbide layer on said diamond substrate for providing a supporting crystal lattice match for wide-bandgap material structures that is better than the crystal lattice match of diamond; and
a Group III nitride heterostructure on said single crystal

silicon carbide layer for providing device characteristics.

[c19] 19. A device according to Claim 18 comprising a poly-crystalline diamond substrate.

[c20] 20. A device according to Claim 18 wherein said silicon carbide layer is semi-insulating.

[c21] 21. A device according to Claim 18 further comprising a Group III nitride buffer layer on said silicon carbide layer for providing a crystal and electronic transition between said heterostructure and said silicon carbide layer.

[c22] 22. A device according to Claim 21 wherein said buffer layer comprises aluminum nitride.

[c23] 23. A device according to Claim 18 wherein said silicon carbide has a polytype selected from the 3C, 4H, 6H and 15R polytypes of silicon carbide.

[c24] 24. A device according to Claim 18 further comprising respective ohmic contacts to said heterostructure.

[c25] 25. A device according to Claim 18 packaged in a high-thermal conductivity material.

[c26] 26. A packaged device according to Claim 25 wherein said high-thermal conductivity material comprises dia-mond.

[c27] 27. A wide-bandgap high electron mobility transistor (HEMT) comprising:
a diamond substrate for providing a heat sink with a thermal conductivity greater than silicon carbide;
a semi-insulating single crystal silicon carbide layer on said diamond substrate for providing a favorable crystal growth surface for Group III nitride epilayers;
a buffer layer on said silicon carbide layer for providing an enhanced crystal transition between silicon carbide and a Group III nitride;
a first epitaxial layer of a first Group III nitride on said buffer layer;
a second epitaxial layer of a different Group III nitride on said first epitaxial layer for forming a heterojunction with said first epilayer, and with said Group III nitride of said second epilayer having a wider bandgap than said first Group III nitride of said first epilayer for generating a two-dimensional electron gas in the first epilayer at the interface of said first and second epilayers; and
respective source, gate, and drain contacts to said second epitaxial Group III nitride layer for providing a flow of electrons between the source and drain that is controlled by a voltage applied to the gate.

[c28] 28. A HEMT according to Claim 27 wherein said first epitaxial layer comprises gallium nitride and said second

epitaxial layer comprises aluminum gallium nitride.

[c29] 29. A HEMT according to Claim 28 wherein said gallium nitride layer is undoped and said aluminum gallium nitride layer is n-doped.

[c30] 30. A HEMT according to Claim 27 wherein said first epitaxial layer comprises gallium nitride and said second epitaxial layer comprises a doped layer of aluminum gallium nitride and an undoped layer of aluminum gallium nitride, with said undoped aluminum gallium nitride layer adjacent said undoped gallium nitride layer.

[c31] 31. A HEMT according to Claim 27 wherein said first epitaxial layer comprises gallium nitride and said second epitaxial layer comprises a layer of aluminum gallium nitride and an undoped layer of aluminum nitride, with said undoped aluminum nitride layer adjacent said undoped gallium nitride layer.

[c32] 32. A HEMT according to Claim 27 packaged in a high thermal-conductivity material.

[c33] 33. A HEMT according to Claim 27 and further comprising a mechanical substrate for said diamond substrate for providing additional mechanical support to said HEMT.

[c34] 34. A HEMT according to Claim 27 wherein said diamond substrate is formed of at least two discrete diamond layers that differ from one another in their properties.

[c35] 35. A HEMT according to Claim 27 wherein said silicon carbide layer is bonded to said diamond substrate.

[c36] 36. A device according to Claim 24 packaged in a high-thermal conductivity material.

[c37] 37. A packaged device according to Claim 32 wherein said high-thermal conductivity material comprises diamond.

[c38] 38. A wide-bandgap high electron mobility transistor (HEMT) comprising:
a diamond substrate for providing a heat sink with a thermal conductivity greater than silicon carbide;
a semi insulating single crystal silicon carbide layer on said diamond substrate for providing a favorable crystal growth surface for Group III nitride epilayers;
a Group III nitride buffer layer on said silicon carbide substrate;
an epitaxial layer of gallium nitride on said buffer layer;
an epitaxial layer of aluminum gallium nitride on said gallium nitride epitaxial layer for forming a heterojunction with said gallium nitride epilayer with said alu-

minum gallium nitride having a wider bandgap than said gallium nitride epitaxial layer for generating a two-dimensional electron gas in said gallium nitride epilayer at the interface of said gallium nitride and aluminum gallium nitride epilayers; and
respective source, gate, and drain contacts to the aluminum gallium nitride layer for providing a flow of electrons between the source and drain that is controlled by a voltage applied to the gate.

[c39] 39. A HEMT according to Claim 38 wherein said gallium nitride layer is undoped and said aluminum gallium nitride layer is n-doped.

[c40] 40. A HEMT according to Claim 38 wherein said buffer layer comprises aluminum nitride.

[c41] 41. A HEMT according to Claim 38 wherein said aluminum gallium nitride layer is formed of a doped layer and an undoped layer, with the undoped aluminum gallium nitride layer adjacent said undoped gallium nitride layer and said ohmic contacts being to said doped layer.

[c42] 42. A HEMT according to Claim 38 wherein said aluminum gallium nitride layer is formed of a doped layer between two undoped layers with one of said undoped layers being adjacent said undoped gallium nitride layer

and the other of said undoped layers being in contact with said respective ohmic contacts.

[c43] 43. A HEMT according to Claim 38 and further comprising a passivation layer above said heterojunction.

[c44] 44. A HEMT according to Claim 38 packaged in a high-thermal conductivity material.

[c45] 45. A packaged device according to Claim 44 wherein said high-thermal conductivity material comprises diamond.

[c46] 46. A wafer precursor for semiconductor devices comprising:
a substrate of single crystal silicon carbide that is at least two inches in diameter; and
a layer of diamond on a first face of said silicon carbide substrate;
wherein the opposite face of said silicon carbide substrate is prepared for Group III nitride epitaxial growth thereon.

[c47] 47. A wafer precursor according to Claim 46 comprising a Group III nitride active structure on said prepared opposite face.

[c48] 48. A wafer precursor according to Claim 46 wherein

said silicon carbide substrate is at least three inches in diameter.

[c49] 49. A wafer precursor according to Claim 46 wherein said silicon carbide substrate is at least 100 mm in diameter.

[c50] 50. A wafer precursor according to Claim 47 wherein said Group III nitride active structure includes at least one heterostructure.

[c51] 51. A wafer precursor according to Claim 50 comprising a buffer layer on said silicon carbide substrate and between said substrate and said heterostructure.

[c52] 52. A wafer precursor according to Claim 46 wherein said silicon carbide has a polytype selected from the group consisting of the 3C, 4H, 6H and 15R polytypes of silicon carbide.

[c53] 53. A wafer precursor according to Claim 46 comprising a plurality of individual active structures on said prepared face of said silicon carbide substrate.

[c54] 54. A semiconductor laser comprising:
a diamond substrate;
a single crystal silicon carbide layer on said diamond substrate;

at least a first cladding layer on said silicon carbide layer;
a Group III nitride active portion on said at least one cladding layer; and
at least a second cladding layer on said active portion.

[c55] 55. A semiconductor laser according to Claim 54 further comprising a buffer layer between said silicon carbide layer and said first cladding layer.

[c56] 56. A semiconductor laser according to Claim 54 comprising a polycrystalline diamond substrate.

[c57] 57. A semiconductor laser according to Claim 54 wherein said silicon carbide has a polytype selected from the 3C, 4H, 6H and 15R polytypes of silicon carbide.

[c58] 58. A method of forming a high power device in wide-bandgap materials with reduced junction temperature, higher power density during operation and improved reliability at a rated power density, the method comprising:
adding a layer of a higher thermal conductivity material to a wafer of lower thermal conductivity material in which the lower thermal conductivity material has a better crystal lattice match with Group III nitrides than does the higher thermal conductivity material to thereby increase the thermal conductivity of the resulting composite wafer;

thereafter reducing the thickness of the lower thermal conductivity portion of the composite wafer while retaining sufficient thickness of the lower thermal conductivity portion to support epitaxial growth thereon;
preparing the lower thermal conductivity surface of the composite wafer for epitaxial growth thereon; and
adding at least one Group III nitride epitaxial layer to the prepared lower thermal conductivity face of the wafer.

[c59] 59. A method according to Claim 58 comprising adding the higher thermal conductivity material from the group consisting of metals, boron nitride and diamond.

[c60] 60. A method according to Claim 58 wherein the lower thermal conductivity material is selected from the group consisting of silicon, gallium nitride, aluminum nitride, aluminum gallium nitride, zinc oxide, lithium aluminate, lithium gallate, magnesium oxide, magnesium aluminate, nickel aluminate and sapphire.

[c61] 61. A method according to Claim 58 wherein the step of adding the at least one Group III nitride epitaxial layer comprises adding at least one Group III nitride heterostructure.

[c62] 62. A method according to Claim 58 wherein the step of adding the higher thermal conductivity material com-

prises growing a polycrystalline layer of diamond.

[c63] 63. A method according to Claim 58 comprising depositing a diamond layer that is thick enough to support the added heterostructure while avoiding additional material that fails to provide further functional benefit.

[c64] 64. A method according to Claim 63 comprising adding a diamond layer that is between about 100 and 300 microns thick.

[c65] 65. A method according to Claim 58 wherein the step of reducing the thickness of the lower thermal conductivity portion comprises lapping and polishing the lower thermal conductivity portion.

[c66] 66. A method according to Claim 58 wherein the step of reducing the thickness of the lower thermal conductivity portion comprises:
implanting the lower thermal conductivity portion at a predetermined depth in the lower thermal conductivity portion to form an implanted layer within the lower thermal conductivity portion prior to the step of depositing the diamond;
thereafter depositing the diamond; and
thereafter reducing the thickness of the lower thermal conductivity portion by separating the lower thermal

conductivity portion at the implanted layer.

[c67] 67. A method according to Claim 66 comprising implanting the lower thermal conductivity portion with oxygen to form an oxide layer and thereafter separating the lower thermal conductivity portion at the oxide layer.

[c68] 68. A method according to Claim 66 comprising implanting the lower thermal conductivity portion with hydrogen and thereafter separating the lower thermal conductivity portion at the hydrogen-implanted layer.

[c69] 69. A method according to Claim 58 comprising depositing the diamond on the lower thermal conductivity portion by chemical vapor deposition.

[c70] 70. A method according to Claim 69 comprising depositing respective first and layers of diamond that differ in properties from one another.

[c71] 71. A method according to Claim 70 comprising: processing the wafer with the second diamond layer and thereafter removing portions of the second layer of diamond.

[c72] 72. A method according to Claim 58 comprising bonding the diamond to the lower thermal conductivity portion.

[c73] 73. A method according to Claim 58 wherein the step of

adding a higher thermal conductivity material comprises adding a metal selected from the group consisting of nickel, tungsten, molybdenum and alloys thereof.

[c74] 74. A high power device in wide-bandgap materials with reduced junction temperature, higher power density during operation and improved reliability at a rated power density, said device comprising:
a layer of a higher thermal conductivity material on one face of a wafer of lower thermal conductivity material in which the lower thermal conductivity material has a better crystal lattice match with Group III nitrides than does the higher thermal conductivity material to thereby increase the thermal conductivity of the resulting composite wafer; and
at least one Group III nitride epitaxial layer on the face of said wafer that is opposite said face with said higher thermal conductivity material.

[c75] 75. A device according to Claim 74 wherein said higher thermal conductivity material is selected from the group consisting of metals, boron nitride and diamond.

[c76] 76. A device according to Claim 74 wherein said lower thermal conductivity material is selected from the group consisting of silicon, gallium nitride, aluminum nitride, aluminum gallium nitride, zinc oxide, lithium aluminate,

lithium gallate, magnesium oxide, magnesium aluminate and nickel aluminate and sapphire.

[c77] 77. A device according to Claim 74 comprising at least one Group III nitride heterostructure.